Vendor:ARM

Exam Code:EN0-001

Exam Name:ARM Accredited engineer

Version: Demo

QUESTION 1

What side-effect could using a debugger to read memory contents have?

A. The memory contents could be set to zero

B. Some memory contents could be rewritten

C. The processor MMU pagetables could be modified

D. The processor cache could be cleaned or/and invalidated

Correct Answer: D

QUESTION 2

When using the default ARM tool-chain libraries for bare-metal applications. I/O functionality is rerouted and handled by a connected debugger. This is often referred to as semihosting. Which one of the following explanations BEST describes how this feature can be implemented by a debugger?

A. The library directly sends I/O requests to the debugger using the JTAG connection

B. While the target is running, the debugger processes I/O requests from a shared queue in memory

C. The I/O library calls rely on an Ethernet connection to redirect the requests to the debugger

D. The I/O library calls generate an exception that is trapped and handled by the debugger

Correct Answer: D

QUESTION 3

When the software floating point emulation library is used, how will the parameters be passed to the following function?

void foo(float f1, float f2, float f3, float f4);

A. On the stack

B. In registers s0-s3

C. In registers d0-d3

D. In registers r0-r3

Correct Answer: D

QUESTION 4

In which of the following scenarios would cache maintenance operations be necessary in an ARMv7 system?

A. Before executing code that uses the NEON instruction set

B. Before handling an interrupt request raised by an external device

C. Before checking the status of a semaphore

D. Before reading cacheable memory that has been written to by an external bus master

Correct Answer: D

QUESTION 5

What type of instruction is used for cache maintenance operations?

A. Dedicated ARM instructions

B. Dedicated Thumb instructions

C. CP14 instructions

D. CP15 instructions

Correct Answer: D

QUESTION 6

Assume a little-endian system.

What is the value of R5 after the execution of the following piece of code?

```
LDR     R1, =0x100
LDR     R2, =0xAABBCCDD
STR     R2, [R1]
ADD     R1, R1, #0x2
LDRB    R5, [R1]
```

A. 0xBB

B. 0xAABBCC22

C. 0x102

D. 0xCC

Correct Answer: A

QUESTION 7

What debugger view can you use to determine which function caused an exception?

A. The Memory view

B. The Variables view

C. The Call Stack view

D. The Breakpoint view

Correct Answer: C

QUESTION 8

How is data written into NOR flash memory?

A. Data can only be written once, when the flash device is being manufactured

B. Writing data to the memory locations using store instruction, as you would with RAM C. Reading and writing specific registers following a device-specific procedure

D. Using an external programming device, which utilizes an ultra-violet lamp to alter the data stored on the device

Correct Answer: C

QUESTION 9

Which of the following techniques can be used to obtain a precise count of clock cycles when profiling software over an arbitrarily long period of time using the Performance Monitoring Unit?

A. A dedicated real-time clock to provide the total cycle count

B. Use of the divide-by 64 counting option to avoid an overflow of the cycle counter

C. Use of the overflow interrupts, to extend the range of the built-in 32-bit counter

D. Modification of the application software being profiled, to insert timestamps at regular intervals

Correct Answer: C

QUESTION 10

Using a lower optimization level when compiling will:

A. Produce faster code.

B. Produce smaller code.

C. Produce non standard-compliant code.

D. Produce code that might be easier to debug.

Correct Answer: D

QUESTION 11

Consider the following piece of code:

```
MOV   r8, #0x00
MSR   CPSR_csfx, #0x13 ;Switch to SVC mode
MOV   r8, #0xAA
MSR   CPSR_csfx, #0x11 ;Switch to FIQ mode
MOV   r8, #0xBB
MSR   CPSR_csfx, #0x13 ;Switch to SVC mode
MOV   r7,r8
```

The value of r7 after execution of the above piece of code is:

A. 0xAA.

B. 0x00.

C. 0xBB.

D. Unpredictable.

Correct Answer: A

QUESTION 12

In a Cortex-A processor, after which TWO of these events is a cache maintenance operation required to ensure reliable code execution? (Choose two)

A. Processor reset

B. Switching from ARM to Thumb state

C. Changing the access permissions of a page

D. Executing a Data Memory Barrier instruction

E. Loading data from an unaligned memory address

Correct Answer: AC